PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H01L 23/64, 23/528 | A2

(11) International Publication Number: WO 00/67320

(43) International Publication Date: 9 November 2000 (09.11.00)

(21) International Application Number: PCT/US00/11798

(22) International Filing Date: 2 May 2000 (02.05.00)

(30) Priority Data:
09/304,137 3 May 1999 (03.05.99) US

(71) Applicant: SILICON WAVE, INC. [US/US]; 6256 Greenwich Drive, Suite 300, San Diego, CA 92122 (US).

(72) Inventors: SEEFELDT, James, Douglas; 4463 Meadowood Circle, DeForest, WI 53532 (US). HULL, Christopher, D.; 6534 Windward Ridge Way, San Diego, CA 92121 (US).

(74) Agents: BERG, Richard, P. et al.; Ladas & Parry, 5670 Wilshire Blvd., Suite 2100, Los Angeles, CA 90036 (US).

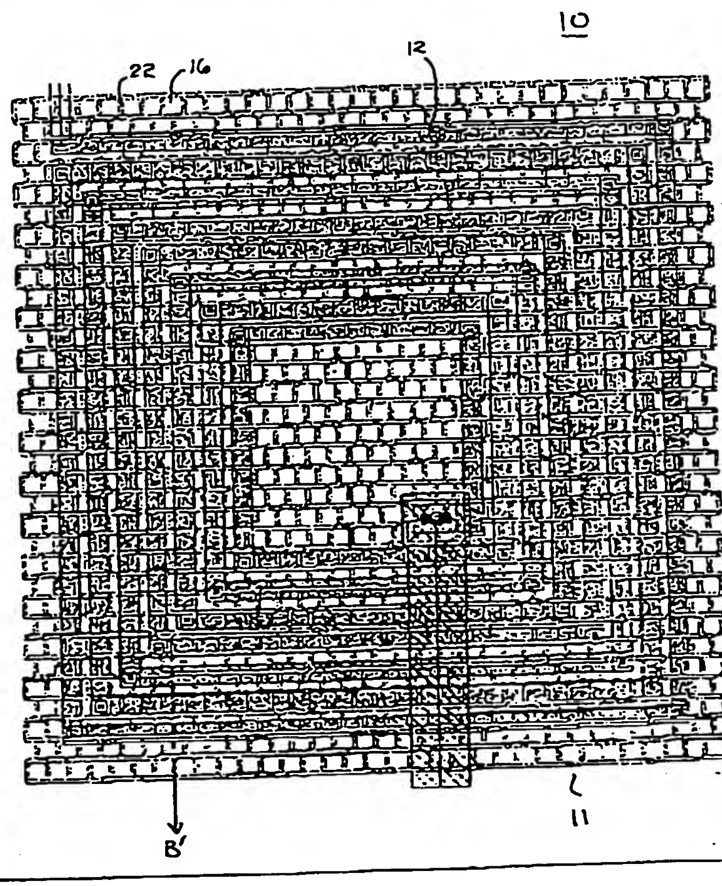
(81) Designated States: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: INTEGRATED CIRCUIT INDUCTOR WITH HIGH SELF-RESONANCE FREQUENCY

(57) Abstract

An integrated circuit inductor structure that includes a shielding pattern that induces a plurality of small eddy currents to shield the magnetic energy generated by the inductor from the substrate of the IC. The IC inductor structure is formed on a Silicon on Insulator (SOI) substrate where the substrate of the SOI has high resistivity. The shielding pattern forms a checkerboard pattern that includes a plurality of conducting regions completely isolated from each other by oxide material. The inductor has a high quality factor and a high self-resonance frequency due to the effective shielding of electromagnetic energy from the substrate of the IC while not reducing the effective inductance of the inductor.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece			TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	NZ	New Zealand		
CM	Cameroon			PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

Integrated Circuit Inductor with High Self-Resonance Frequency

BACKGROUND OF THE INVENTION

1. *Field of the Invention*

This invention relates to integrated circuit inductors and more particularly to integrated circuit inductors having a high self-resonance frequency and a high quality factor, Q_n.

2. *Description of Related Art*

It is desirable to include inductors on integrated circuits ("IC") versus off the IC to reduce the form factor and cost of devices requiring inductors. IC inductors, however, commonly have unacceptably low quality factors, low self-resonance, and cause interference with surrounding or neighboring IC components. This is particularly true for IC inductors used in high frequency applications such as in the front end of radio frequency ("RF") receivers and transmitters.

Due to the significant advantages of having IC inductors, several solutions have been investigated. First, inductors having different geometric patterns such as those shown in FIGURES 1A to 1C have been analyzed including a spiral inductor 42, a simple loop inductor 44, and a meander inductor 46. Of these inductors, investigation has revealed that spiral inductors are most easily adapted for inclusion in silicon ICs because a desired inductance can be achieved using a smaller surface area with a spiral inductor versus a loop or a meander inductor.

As way of background FIGURE 2A shows such an inductor 50 which generates magnetic field lines 52 due to the flow of current shown in the FIGURE. FIGURE 2B illustrates a cross sectional view of an IC structure 54 including the inductor 50. The IC 54 includes a silicon substrate 56, a conductive ground plane 58, and a silicon oxide layer 60. When the inductor 50 is included on an IC such as shown in FIGURE 2B and current flows through the inductor 50 such as shown in FIGURE 2A, the lines of magnetic field can enter the substrate 56 and be significantly reduced. This reduces the quality factor (Q_n) of the inductor. In addition the frequency at which the inductor 50 self-resonances is also reduced due to parasitic capacitance between the inductor 50 and the substrate 56.

In order to limit the passage of the magnetic fields of an inductor into the IC's substrate, insulating regions and ground plates have been inserted between the inductor and substrate. For example, U.S. Pat. No. 5,539,241 to Abidi et al. teaches etching a pit under the inductor to create an insulating region between the inductor and the substrate. As noted in the PCT application number US98/05149 to Yue et al. (which is discussed below), the inclusion of this insulating region may effect the mechanical integrity of the IC, in particular, the inductor. In addition, the construction of an IC with such insulating region is likely to be expensive and complex.

Yue et al. also discusses another IC inductor structure where the structure includes a solid metal conducting ground shield 72 such as shown in FIGURE 3A. As shown in FIGURE 3B, the solid conducting ground shield 72 is placed between the inductor 50 and the substrate 56. As shown in FIGURE 3A, an image current 76 is induced from the magnetic field lines generated by the inductor 50. This induced image current 76 generates magnetic field lines 74 where the flux of the magnetic field is opposite the flux of the magnetic field of the inductor 50. Consequently, while this IC inductor configuration isolates the inductor 50 from the substrate 56 (no magnetic coupling), the configuration substantially reduces the effective inductance of the inductor and thereby the Q_n of the inductor.

In order to overcome these problems, Yue et al. suggests an IC inductor configuration that includes a patterned ground shield 80 between the inductor 50 and substrate 56 as shown in FIGURES 4A and 4B. The patterned ground is a polysilicon ground shield that includes locally isolated conductive lines 84 separated by slots 85 where the conductive lines 84 are orthogonal to the conductive line segments of the inductor 50. Yue et al. teaches that the orthogonal relationship between the conductive lines 84 and conductive line segments reduces or eliminates the generation of an image current in the ground shield 80. The ground shield effectively terminates any electric field generated by the inductor 50 thus limiting any leakage into the substrate 56. The termination of the electric field at the ground shield 80, however, may effectively generate a quasi capacitor where the inductor acts as one plate and the ground shield acts as another plate. The relative proximity of the inductor to the ground shield increases its effective capacitance. Consequently, the IC inductor configuration of Yue et al. may not have an acceptable quality factor at high frequencies.

It is also noted that Yue et al. suggests that the substrate 56 is a low resistivity substrate. In particular, Yue et al. includes examples of an 11 ohm-cm silicon substrate and a 19 ohm-cm silicon substrate. It has been found that low resistivity substrates employed in IC inductor configurations may also lower the self-resonance frequency of the inductor regardless of the ground shield or grounding technique employed. Thus, a need exists for an IC inductor configuration that has a high self-resonance frequency and an acceptable quality factor at high frequencies.

SUMMARY OF THE INVENTION

The present invention is an integrated circuit inductor structure that includes a shielding pattern that induces a plurality of small eddy currents to shield magnetic energy generated by the inductor from the substrate of the IC. The IC inductor structure is formed on a Silicon on Insulator (SOI) substrate where the substrate of the SOI has high resistivity. The shielding pattern forms a checkerboard pattern that includes a plurality of conducting regions completely isolated from each other by a dielectric or non-conducting material. The inductor has a high quality factor and a high self-resonance frequency due to the effective shielding of electromagnetic energy from the substrate of the IC while not reducing the effective inductance of the inductor or introducing substantial parasitic capacitance.

In other embodiment, the IC inductor structure includes an inductor formed over a second dielectric layer. The second dielectric layer is formed over a first dielectric layer and the first dielectric layer is formed over a substrate. The substrate ideally has high resistivity. In particular, the resistivity is about 1 kohm-cm. The first dielectric layer is formed from silicon oxide and the second dielectric layer is formed from at least one oxide layer. In another embodiment, a plurality of conducting regions are inserted into the second dielectric layer wherein the plurality of conducting regions induce small eddy currents that do not significantly reduce the inductance of the inductor.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1A is a diagram of an exemplary prior art spiral inductor.

FIGURE 1B is a diagram of an exemplary prior art loop inductor.

FIGURE 1C is a diagram of an exemplary prior art meander inductor.

FIGURE 2A is a perspective view of a prior art spiral inductor and lines of magnetic fields generated by the same when current circulates through the inductor.

FIGURE 2B is a cross sectional view of a prior art IC inductor structure where the inductor is a spiral inductor and the structure has no grounding shields or shielding patterns.

FIGURE 3A is a perspective view of a prior art solid metal ground shield and lines of magnetic fields generated by the same when current circulates through the shield.

FIGURE 3B is a cross sectional view of a prior art IC inductor structure where the inductor is a spiral inductor and the structure has includes the solid metal ground shield shown in FIGURE 3A.

FIGURE 4A is a top view of a prior art spiral inductor over a patterned ground shield.

FIGURE 4B is a cross sectional view of a prior art IC inductor structure including the spiral inductor and patterned ground shield shown in FIGURE 4A.

FIGURE 5 is a top view of a spiral inductor over a patterned shield in accordance with the present invention where the patterned shield forms a checkerboard pattern of isolated conducting regions.

FIGURE 6 is a diagram of a section BB' of the spiral inductor over a patterned shield as shown in FIGURE 5.

FIGURE 7 is a cross section AA' of the spiral inductor over the patterned shield as shown in FIGURE 6 where the cross section details a first embodiment of an IC inductor structure according to the present invention.

FIGURE 8 is a cross section AA' of the spiral inductor over the patterned shield as shown in FIGURE 6 where the cross section details a second embodiment of an IC inductor structure according to the present invention.

FIGURES 9A to 9D are graphs detailing the ratio of inductor quality, Q_n versus operating frequency, f_n for different IC inductor structures.

FIGURE 10 is a cross sectional view of the first embodiment of an IC inductor structure according to the present invention shown in FIGURE 7 further surrounded by a guard ring structure to electrically isolate the IC inductor from neighboring IC components.

FIGURES 11 to 15 are sectional views of an exemplary method of producing or manufacturing the IC structure shown in FIGURE 10.

Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION OF THE INVENTION

Throughout this description, the preferred embodiment and examples shown should be considered as exemplars, rather than as limitations on the present invention.

As noted above, an ideal IC inductor configuration has a high quality factor at high frequencies and a high self-resonance frequency. An exemplary IC inductor configuration 10 according to the present invention is presented with reference to FIGURES 5 to 7. FIGURE 5 is a top-level view of an exemplary IC inductor configuration 10 according to the present invention. The IC 10 includes an inductor 12 over a checkerboard pattern 11 that includes a plurality of conducting regions 16 isolated at four sides by isolating lines 22. FIGURE 6 is a diagram of section BB' of the IC 10 shown in FIGURE 5. FIGURE 6 more clearly illustrates the conductive regions 16 that are electrically isolated from each other by isolating lines 22. The combination of conductive regions 16 and isolating lines 22 form a checkerboard pattern 11 of electrically isolated conducting regions 16.

In use, the inductor 12 generates magnetic field lines that enter each of the conducting regions 16. The magnetic field lines induce small eddy currents in each of the conducting regions 16 since the regions are not grounded as in the Yue et al. configuration described above. Due to the small size of the conducting regions and their isolation from other conducting regions 16 (the isolation is shown in more detail in FIGURES 7 and 8), a magnetic field having a flux opposite of the flux of the magnetic field generated by the inductor 12 is not induced. Consequently, the inductance of the inductor 12 is not reduced. FIGURE 7 is diagram of an exemplary side section AA of IC 10 shown in FIGURE 6.

The exemplary side section of IC 10 includes a high resistivity substrate 20, silicon oxide layer 18, shield region 11 comprised of epitaxial silicon 16 and an oxide 22, an oxide layer 14 and an inductor pattern 12. In this preferred embodiment, the inductor 12 is formed on a Silicon On Isolator ("SOI") pattern. It is noted that ideally the substrate 20 has a resistivity of about 1 kohm-cm. As shown in this FIGURE, each conducting region 16 is comprised of epitaxial silicon which is separated from neighboring regions by U-trenches 22 filled with a non-conductive oxide. Between the inductor 12 and the conducting regions is an oxide layer 14. The oxide layer 14 may be comprised of one or more different oxide layers. The SOI is ideally formed over a conducting Printed Circuit Board ("PCB") 21.

Accordingly, when a current flows in inductor 12, small eddy currents are generated in each epitaxial region 16. As noted, these regions 16 are not grounded. Consequently, an electric field signal is generated that is electrically grounded at the PCB 21 level. This creates a small effective capacitor where the inductor 12 acts as the first plate and the PCB 21 acts as the second plate. Due to the distance between the inductor 12 and PCB 21, the effective capacitance of such a capacitor is small. Accordingly, the IC inductor configuration 10 according to the present invention has a high quality factor and a high self-resonance frequency (as shown in FIGURES 9A to 9D, which are presented below). FIGURE 8 is a cross sectional diagram of another exemplary IC inductor configuration 30 according to the present invention. In this configuration 30, each conducting region of the checkerboard pattern includes a n-type collector ("CN") region 24 and n-type buried layer ("NBL") region 26. These regions have a lower resistance than an undoped epitaxial silicon. Consequently, the IC inductor configuration 30 may have a higher quality factor.

FIGURES 9A to 9D illustrate the quality factor, Q_n versus operating frequency, f_n for different IC inductor configurations. The inductor configurations modeled in FIGURES 9A and 9B have low resistivity substrates 20 while the inductor configurations modeled in FIGURES 9C and 9D have high resistivity substrates 20 as in the preferred embodiments. In addition, the inductor configurations modeled in FIGURES 9B and 9C include the checkerboard isolation regions as shown in FIGURES 5 to 8, while the inductor configurations modeled in FIGURES 9A and 9D do not include the checkerboard isolation regions. As can be seen by review of these figures, the IC inductor configuration that includes a high resistivity substrate with checkerboard isolation region has the highest quality factor and also the highest self-resonance (the high point of the quality factor occurs at the highest operating frequency). These FIGURES also indicate that the inclusion of a high resistivity substrate greatly increases the quality factor and self-resonance frequency of the IC inductor.

It is also noted that the isolation technique according to the present invention also helps to isolate the inductor 12 from neighboring IC components. In high frequency applications, higher isolation techniques may be required. FIGURE 10 is a cross sectional diagram of an exemplary structure that isolates an inductor 12 according to the present invention. In this FIGURE, the IC inductor configuration 10 is isolated by a guard ring configuration that is described in detail in the co-pending and commonly assigned application entitled "Trench Isolated Guard Ring Region for Providing RF Isolation" filed February 23, 1999 and assigned application number 09/255,747. This application is hereby incorporated by reference for its teachings on guard ring region isolation techniques.

As shown in FIGURE 10, the IC inductor 10 is inserted in a mesa formed by a guard ring including by U-trenches 23 immediately surrounding the inductor configuration 10. Each U-trench 23 has adjacent CN 36 and NBL 38 conductive regions coupled by a metal contact 32 to a ground 34. The conductive regions are also surrounded by U-trenches. As described in the co-pending and incorporated application, the guard ring isolation configuration further isolates the IC inductor configuration 10 from neighboring IC components.

As noted above, the IC inductor configuration 10 according to the present invention ideally uses Silicon-On-Insulator (SOI) as its base. As shown in FIGURES 5 to 8, and 10. an insulating layer 18 separates circuit devices 12 from the solid silicon substrate 20. The advantages of SOI BiCMOS process technology include greater signal isolation, higher speed devices with lower power consumption, and dense digital CMOS logic. The circuitry of the present invention is preferably implemented in an SOI BiCMOS process technology that uses bonded wafers ("bonded SOI"). Bonded SOI processes are well known to those of ordinary skill in the art and are believed to be currently available. Examplary SOI BiCMOS process technologies that may be used to implement the inventive inductor structure are described in U.S. Patent No. 5,661,329 entitled "Semiconductor Integrated Circuit Device Including An Improved Separating Groove Arrangement", U.S. Patent No. 5,773.340 entitled "Method of Manufacturing a BIMIS", and U.S. Patent No. 5,430,317 entitled "Semiconductor Device", the complete disclosures of which are all hereby fully incorporated into the present application by reference.

A process for producing the IC inductor 40 shown in FIGURE 40 on an SOI base is described with reference to FIGS. 11 to 15. As shown in FIGURE 11, the SOI substrate is formed by growing an oxide (SiO2), layer 20, on the surface of an N type silicon wafer, layer 38. The resultant silicon wafer is bonded to another silicon wafer, layer 18, with the SiO2 layer, layer 20, in between the two silicon layers, layers 38 and 18. Then, the original N type wafer, layer 38, is polished down until a thin, approximately .5um, layer remains. This sandwich 18. 20, 38 now forms the SOI substrate. As shown in FIGURE 12, an N-type region is formed by masking the substrate and implanting and driving, by thermal diffusion, an N type impurity into layer 38 (The NBL layer , 40, is not needed with the trench grid structure). An N type epitaxial layer, layer 48, is then grown on top of layer 38 and layer 40.

As shown in FIGURE 13, an insulation oxide layer, layer 50, is grown on top of layer 48 by means of thermal oxidation. Next, a masking pattern is formed by means of exposing and developing photoresist on top of layer 50. The masking pattern can either be a trench grid or a radial type trench structure, which is used to prevent eddy current formation in the layers 38 and 48. Narrow trenches, 55, are formed by RIE etching through the oxide layer 50 and the silicon layers, layers 48, 38 and 40, down to the insulating oxide layer, layer 18. As shown in Figure 14, the trenches are filled with CVD oxide, which conformally fills and closes the trenches. The CVD layer is removed from the surface of the wafer but remains in the trenches, 57. The metalization layers that form the inductor 12 can now be fabricated on top of the trench structure. As shown in Figure 15, an insulating SiO2 layer, layer 60, is deposited on top of layer 50 and layer 57. This is followed by a metalization layer, layer 68, in which the inductor 12 is formed. The metalization layer could be fabricated from Al, AlSi, AlSiCu, Cu, or any suitable conducting material. This could be followed with more layers of insulators, such as layer 70, and additional metal layers, such as layer 78. The metal layers may be connected by means of another layer 75, patterned and etched between the metal layers. Multiple layers of metal can be used to form the inductor in order to reduce the series resistance of the inductor.

It is noted that variations of the above techniques are possible. In particular, the checkerboard pattern 11 may be used in other IC inductor structures that do not employ SOI processing. In addition, an IC inductor structure may be formed using SOI without a checkerboard pattern that performs well provided the substrate has high resistivity. Thus, numerous modifications may be made to the IC inductor configuration described in this specification. Consequently, the invention is not to be limited by the specific illustrated embodiment, but only by the scope of the appended claims.

CLAIMS

What is claimed is:

1. An integrated circuit comprising:
   a) a high resistivity substrate;
   b) a first dielectric layer contacting the substrate at an interface;
   c) a second dielectric layer contacting the first dielectric substrate at an interface; and
   d) an inductor fabricated above the second dielectric layer.

2. The integrated circuit according to claim1, wherein the resistivity of the substrate is about 1 kohm-cm.

3. The integrated circuit according to claim 1, wherein the first dielectric layer consists of silicon oxide.

4. The integrated circuit according to claim 3. wherein the second dielectric layer includes at least one oxide layer.

5. An integrated circuit comprising:
   a) a substrate;
   b) a first dielectric layer contacting the substrate at an interface;
   c) a plurality of conducting regions located within a second dielectric layer wherein the plurality of conducting regions induce small eddy currents that do not significantly reduce the inductance of the inductor
   d) a third dielectric layer contacting the second dielectric layer at an interface; and
   e) an inductor fabricated above the second dielectric layer.

6. The integrated circuit according to claim 5, wherein the substrate is a high resistivity substrate.

7. The integrated circuit according to claim 6, wherein the resistivity of the substrate is about 1 kohm-cm.

8. The integrated circuit according to any one of claims 5 - 7, wherein the first dielectric layer consists of silicon oxide.

9. The integrated circuit according to any one of claims 5 - 8, wherein the second dielectric layer includes at least one oxide layer.

10. A method of making integrated circuit on a substrate, the method comprising:

a) forming a array of conducting regions in said substrate, said conducting regions being spaced from one another by dielectric;

b) forming a dielectric layer contacting the substrate at an interface; and

c) forming an inductor above the dielectric layer.

11. The method according to claim 10, wherein the substrate is a high resistivity substrate.

12. The method according to claims 10 or 11, wherein the resistivity of the substrate is about 1 kohm-cm.

13. The method according to any one of claims 10 - 12, wherein the dielectric between the conducting regions of silicon oxide.

14. The method according to any one of claims 10 - 13, wherein the second dielectric layer includes at least one oxide layer.

15. The method according to any one of claims 10 - 14, wherein the array of conducting regions forms a checkerboard pattern.

42

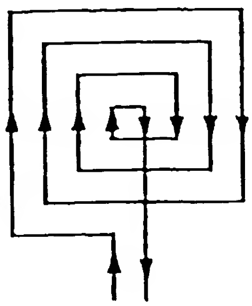


FIG. 1A
(PRIOR ART)

44

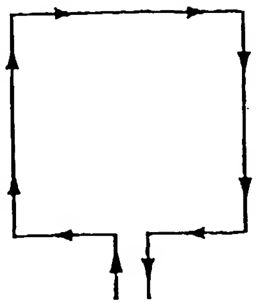


FIG. 1B
(PRIOR ART)

46

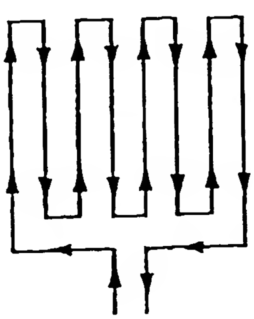


FIG. 1C
(PRIOR ART)

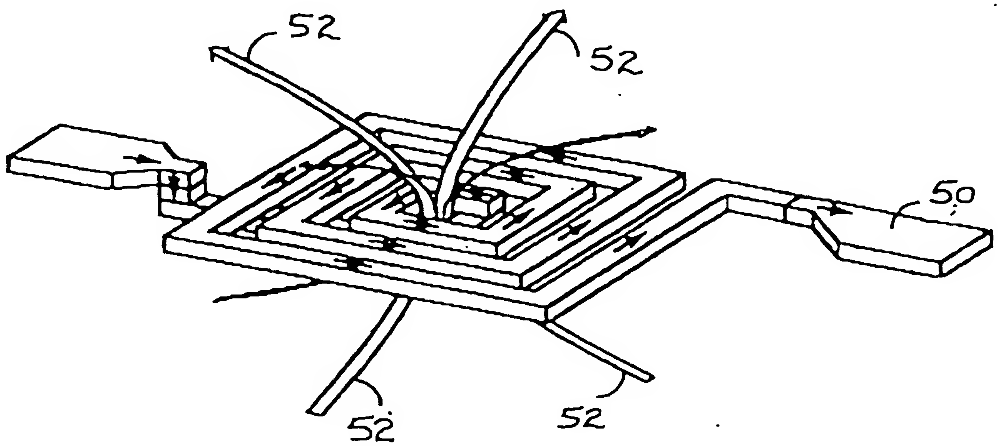


FIG. 2A
(PRIOR ART)

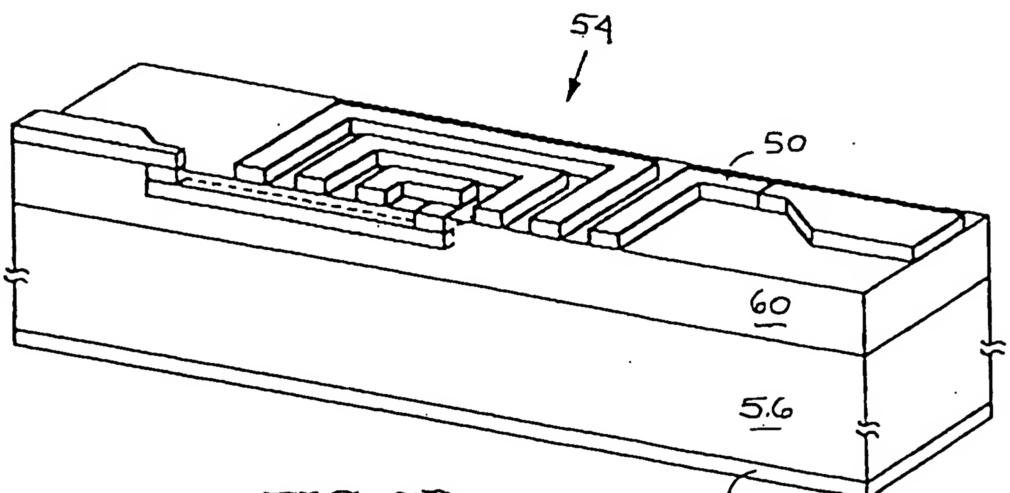


FIG. 2B
(PRIOR ART)

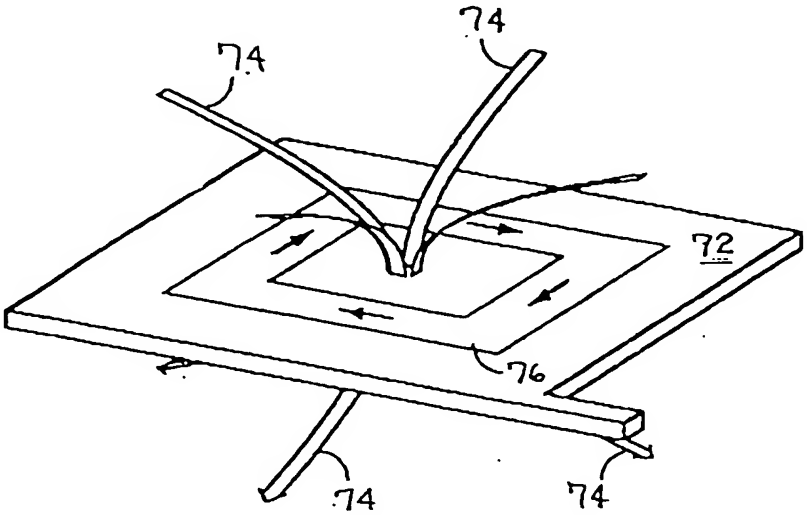


FIG. 3A
(PRIOR ART)

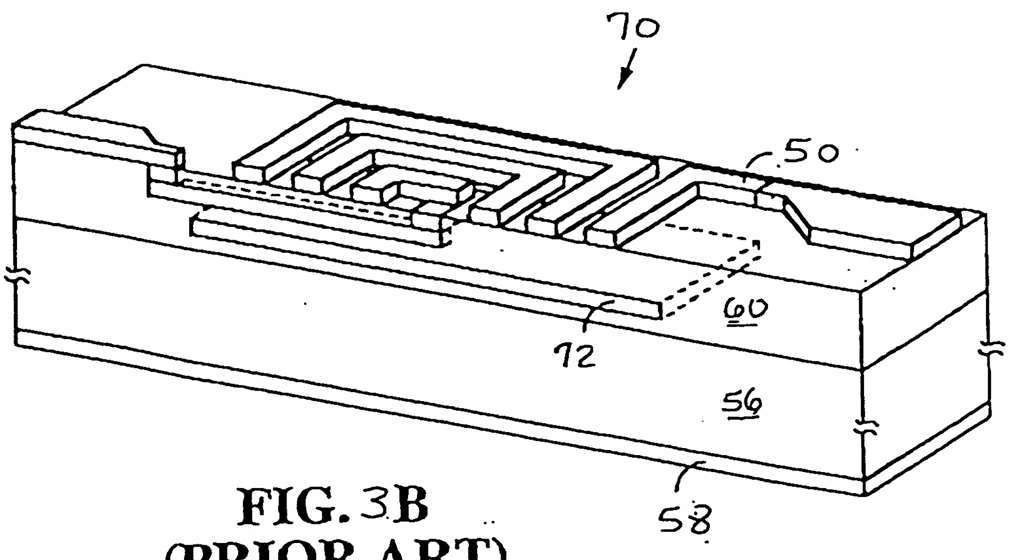


FIG. 3B
(PRIOR ART)

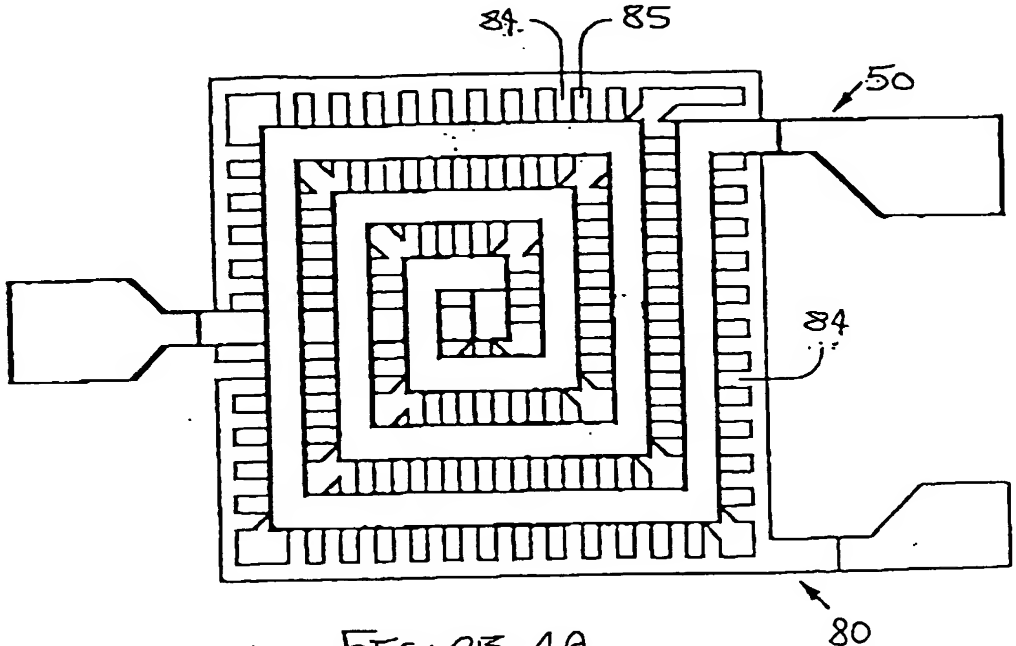


FIGURE 4A
(PRIOR ART)

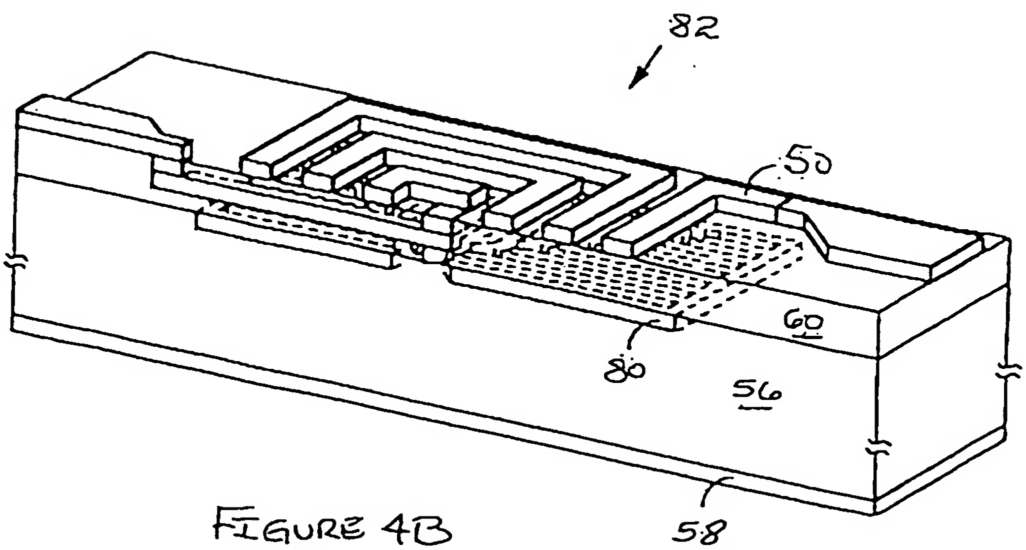


FIGURE 4B
(PRIOR ART)

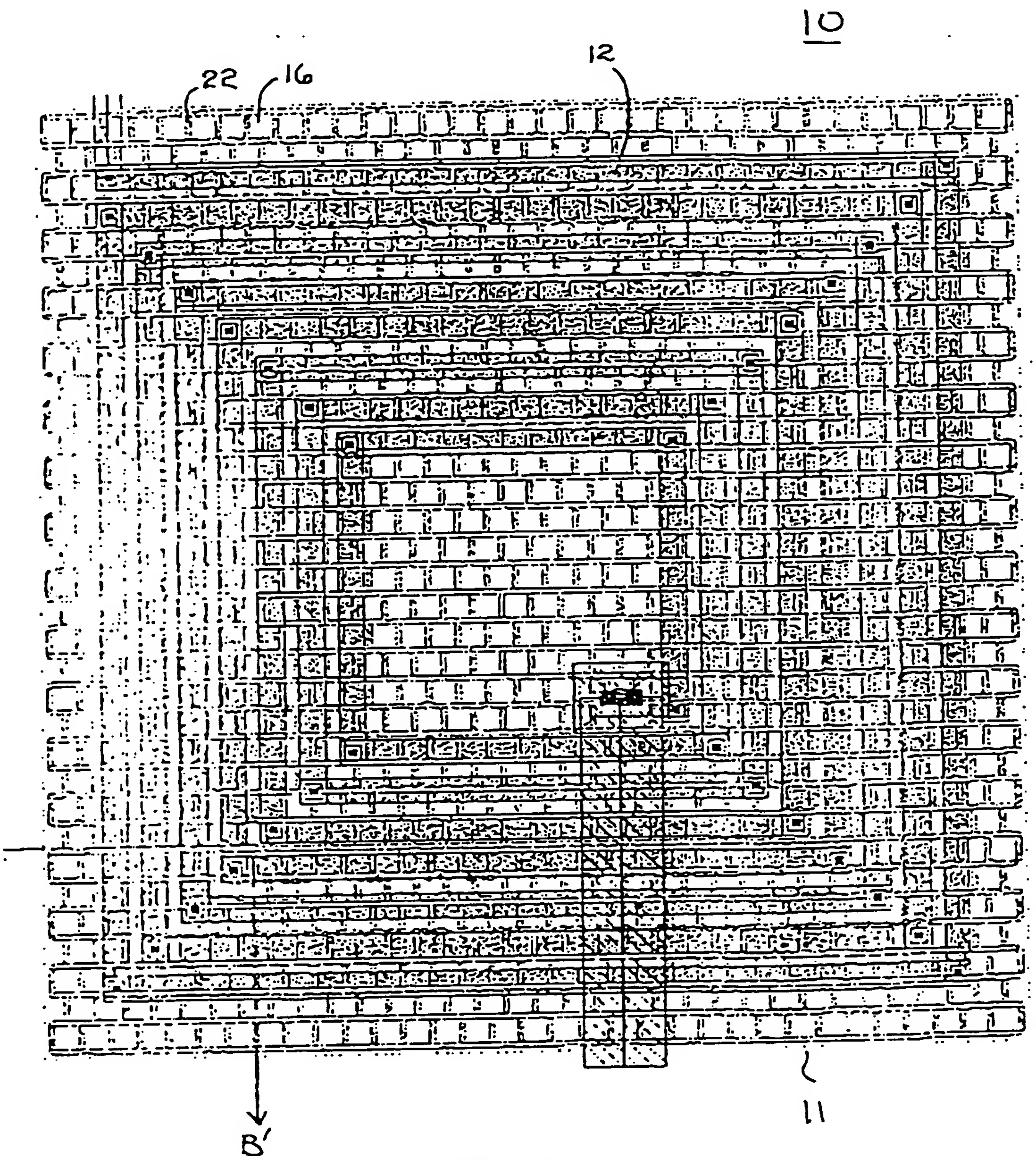


FIGURE 5

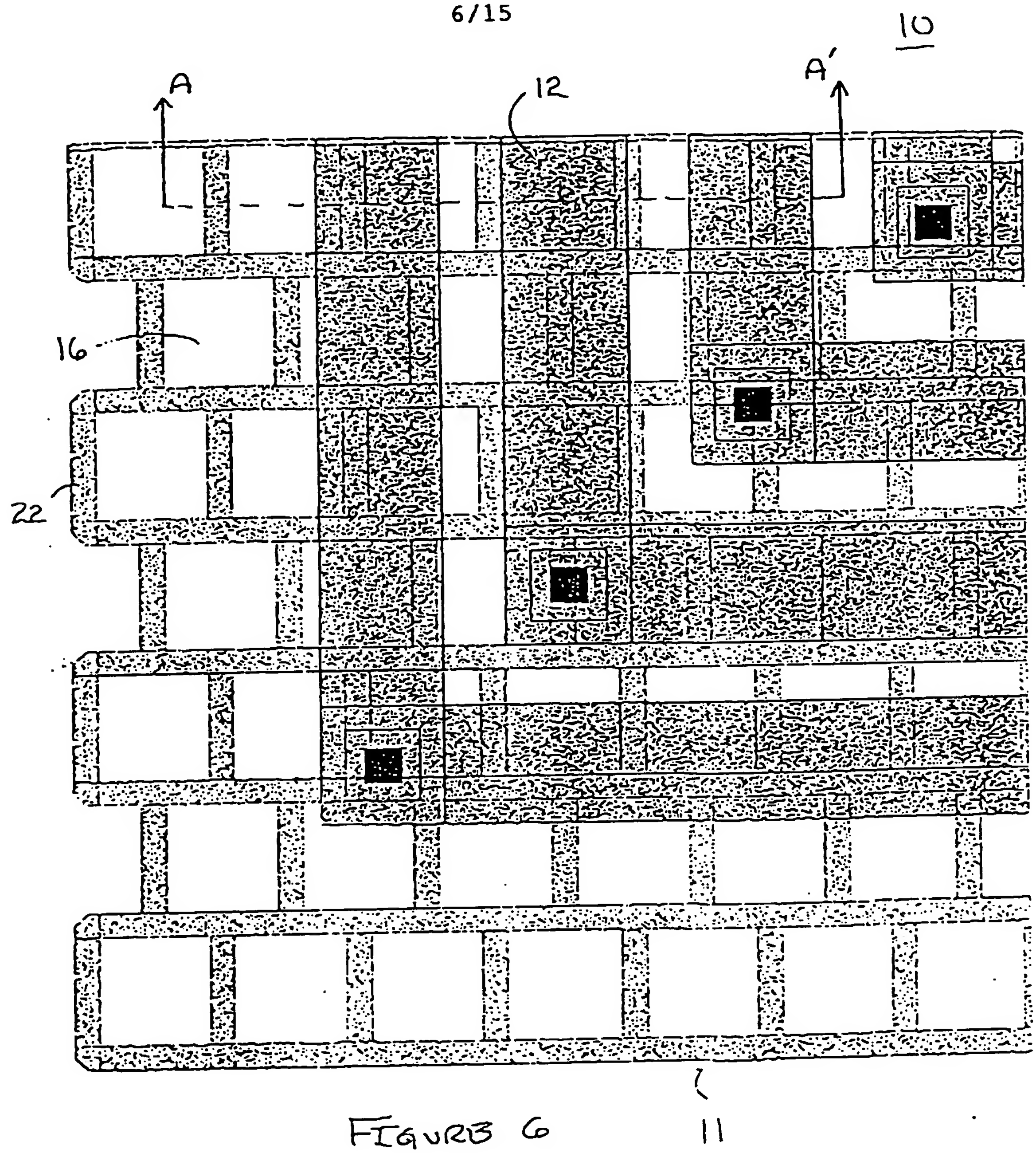


FIGURE 6

FIGURE 7

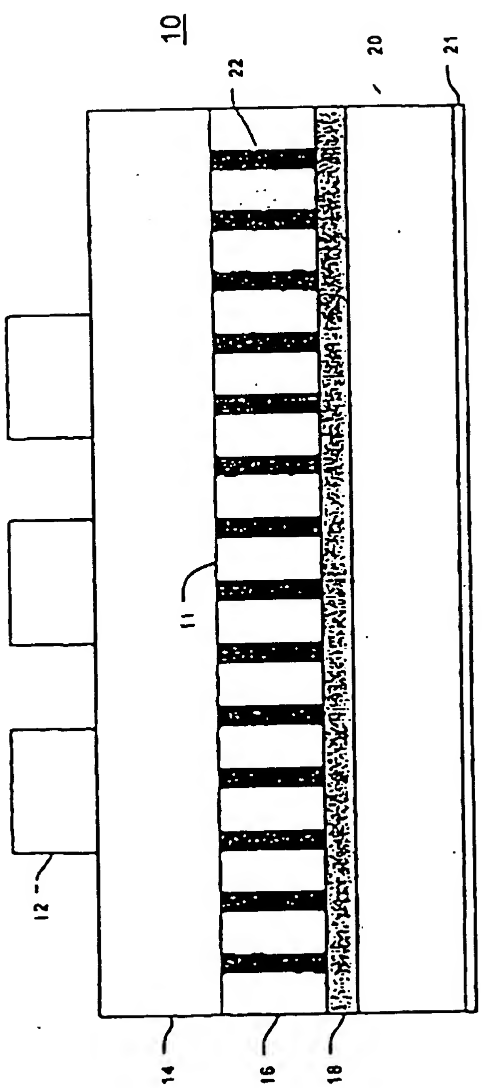
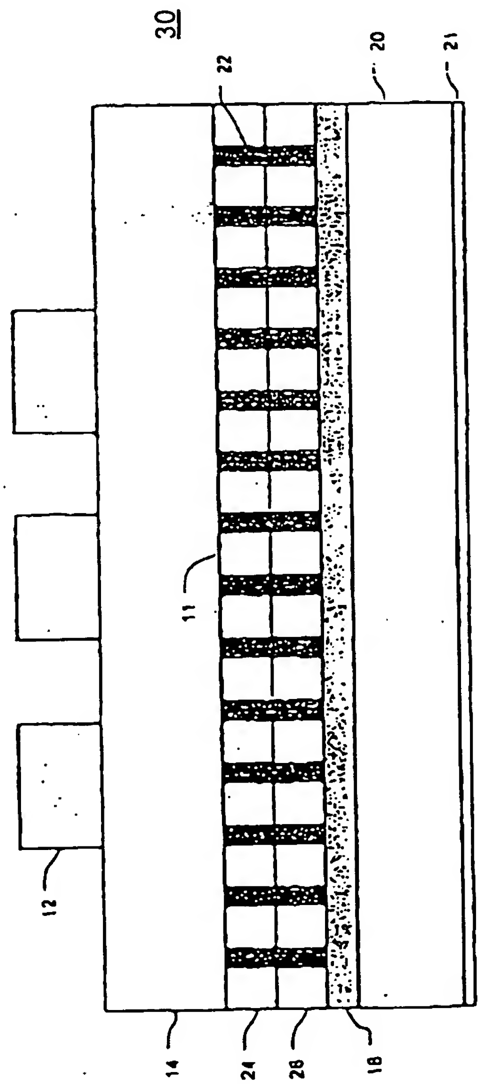


FIGURE 8



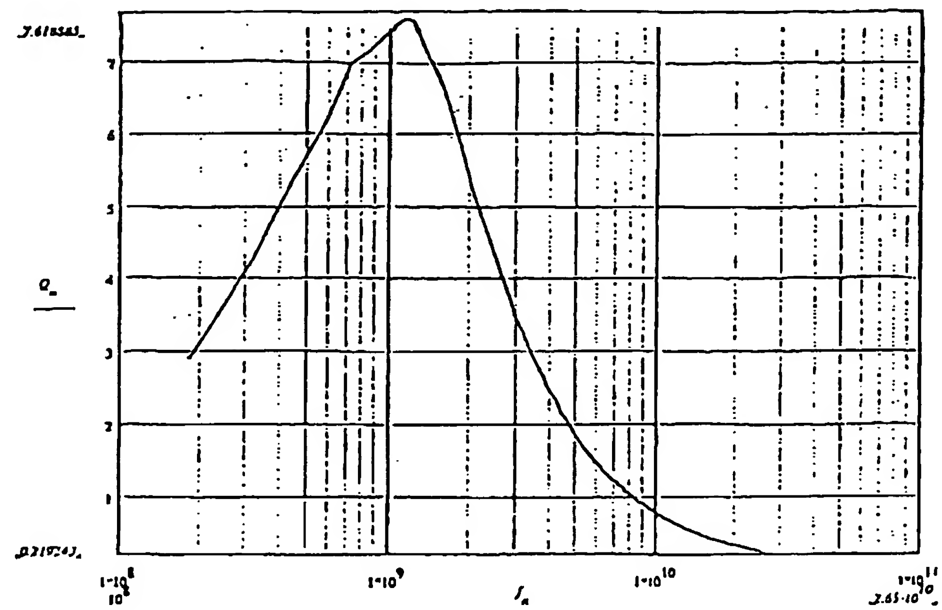


FIGURE 9A

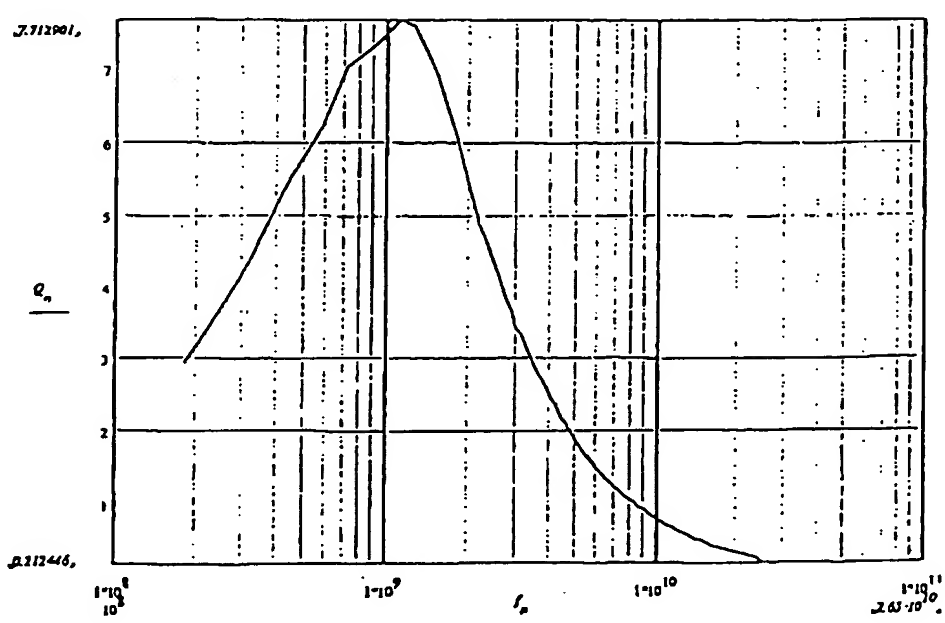


FIGURE 9B

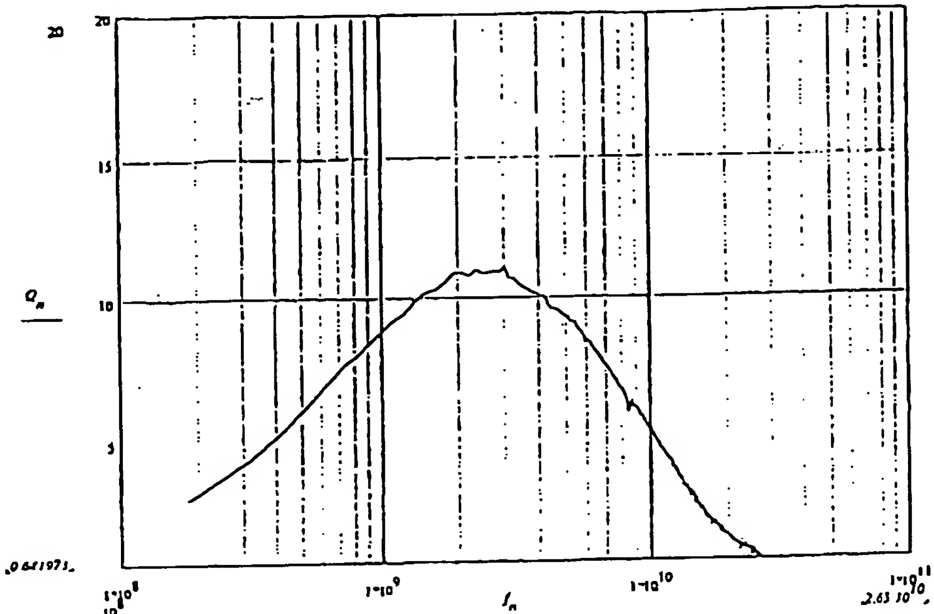


FIGURE 9C

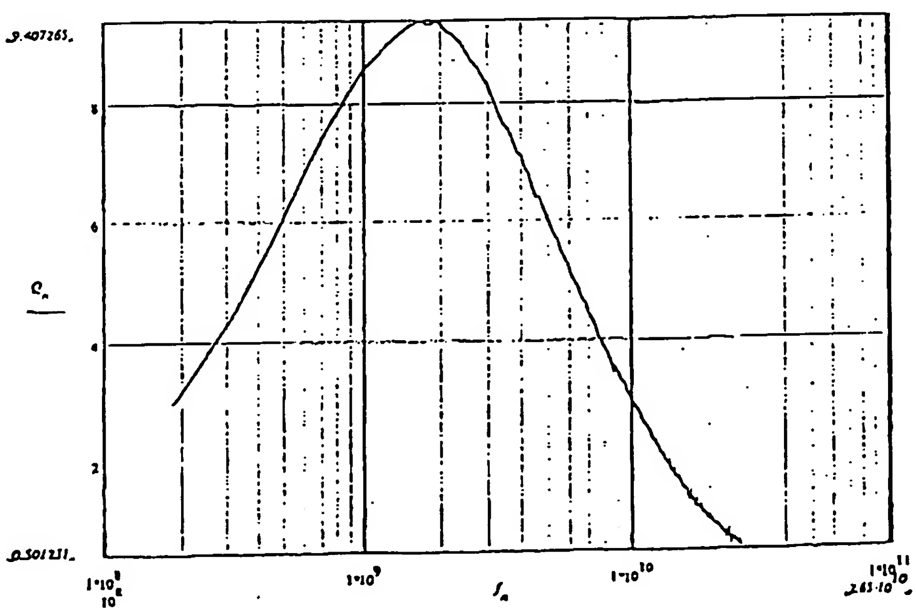


FIGURE 9D

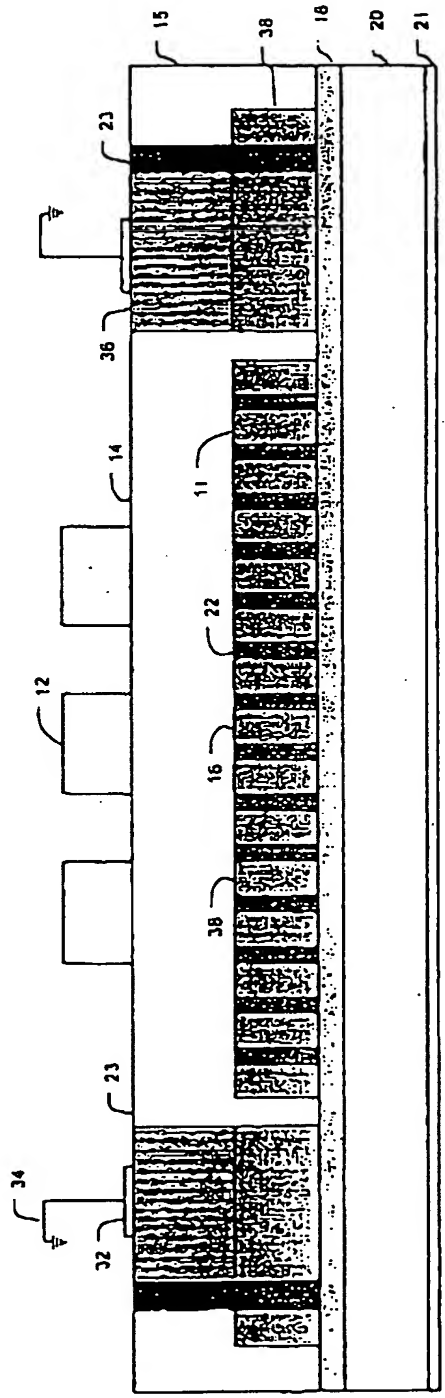


FIGURE 10

40

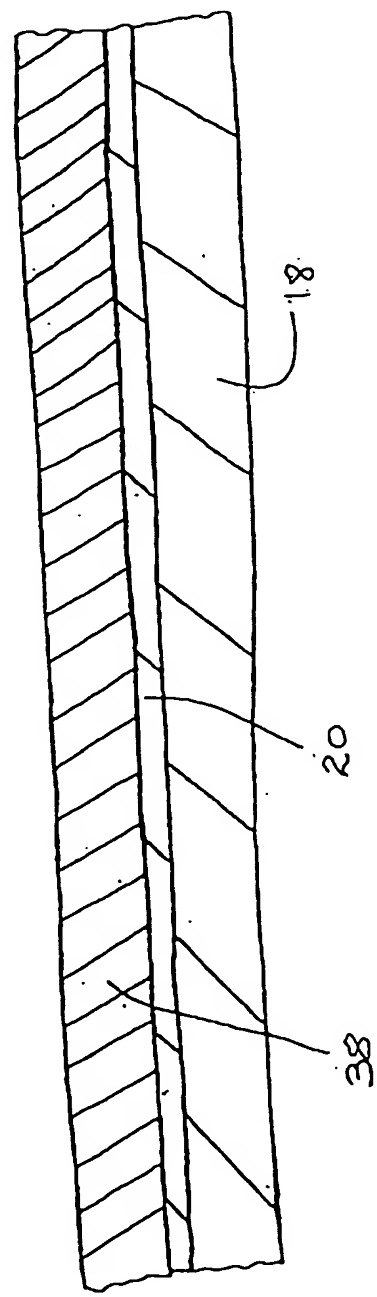


FIG. 11

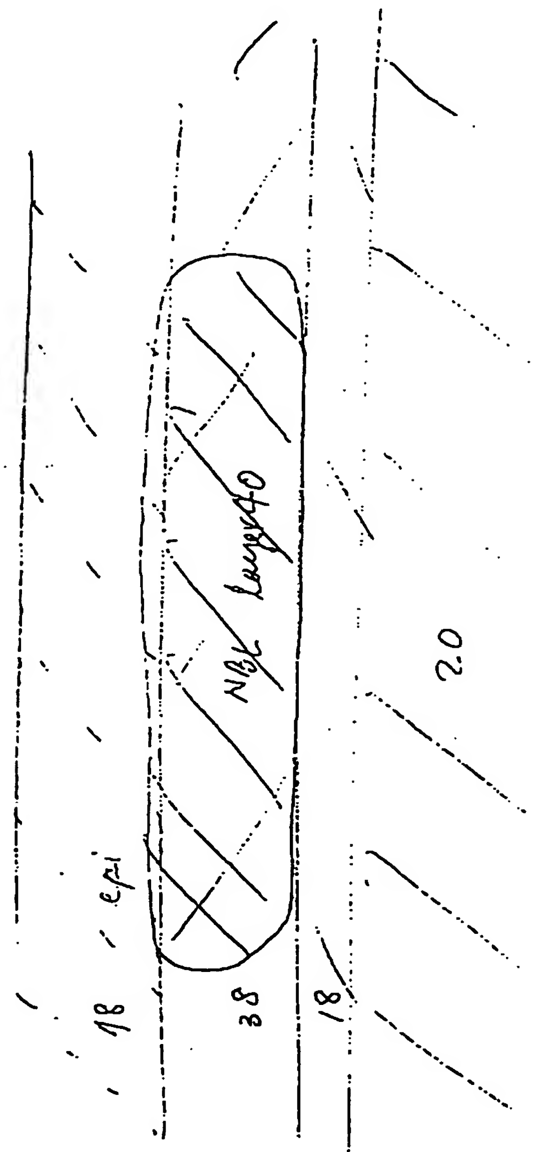


Fig 12

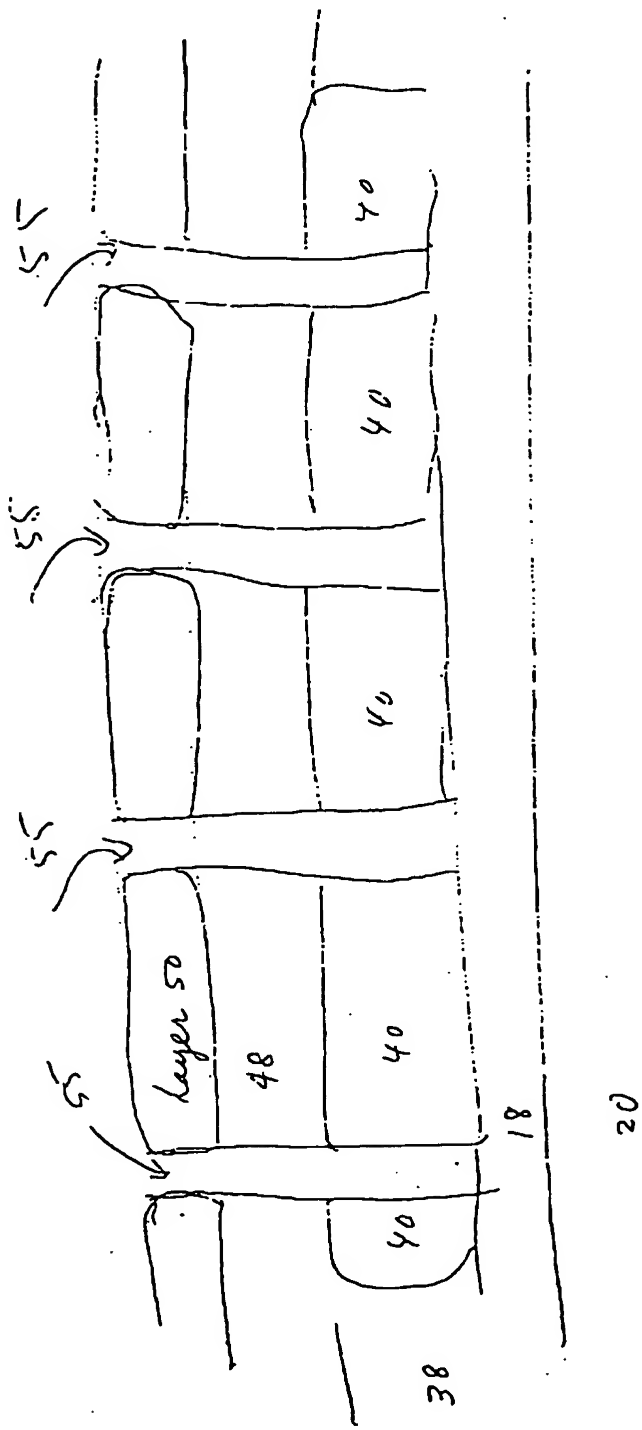


FIGURE 13

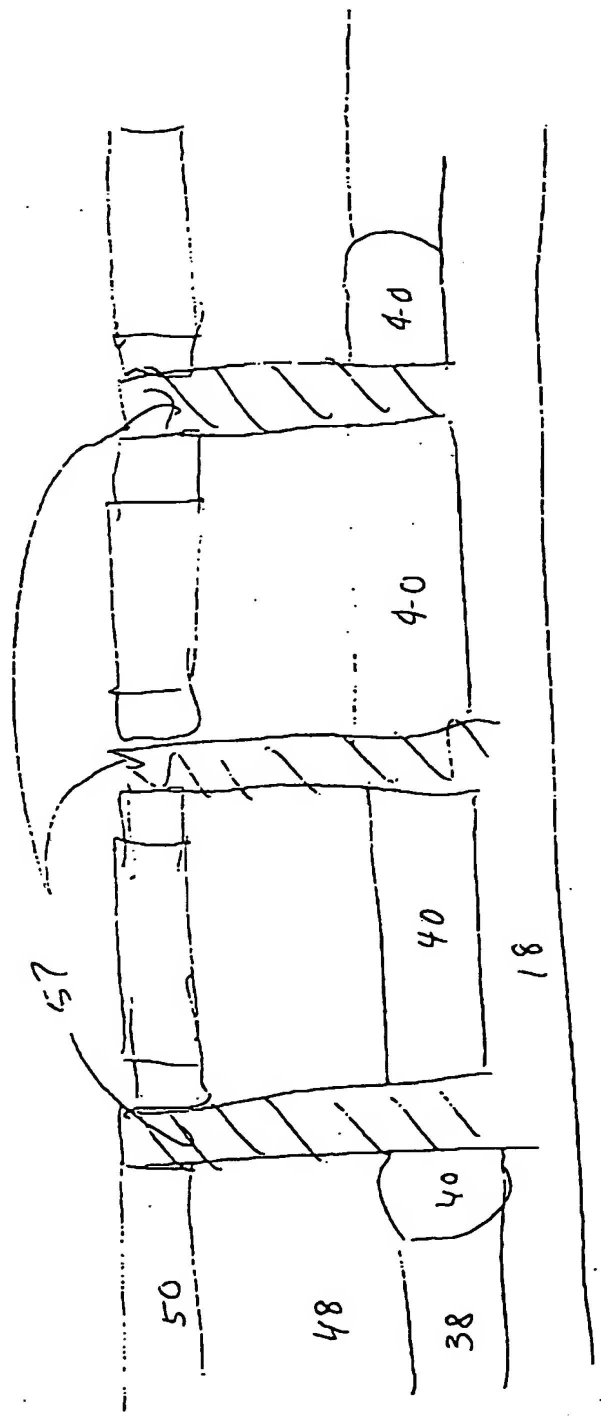


Fig 14

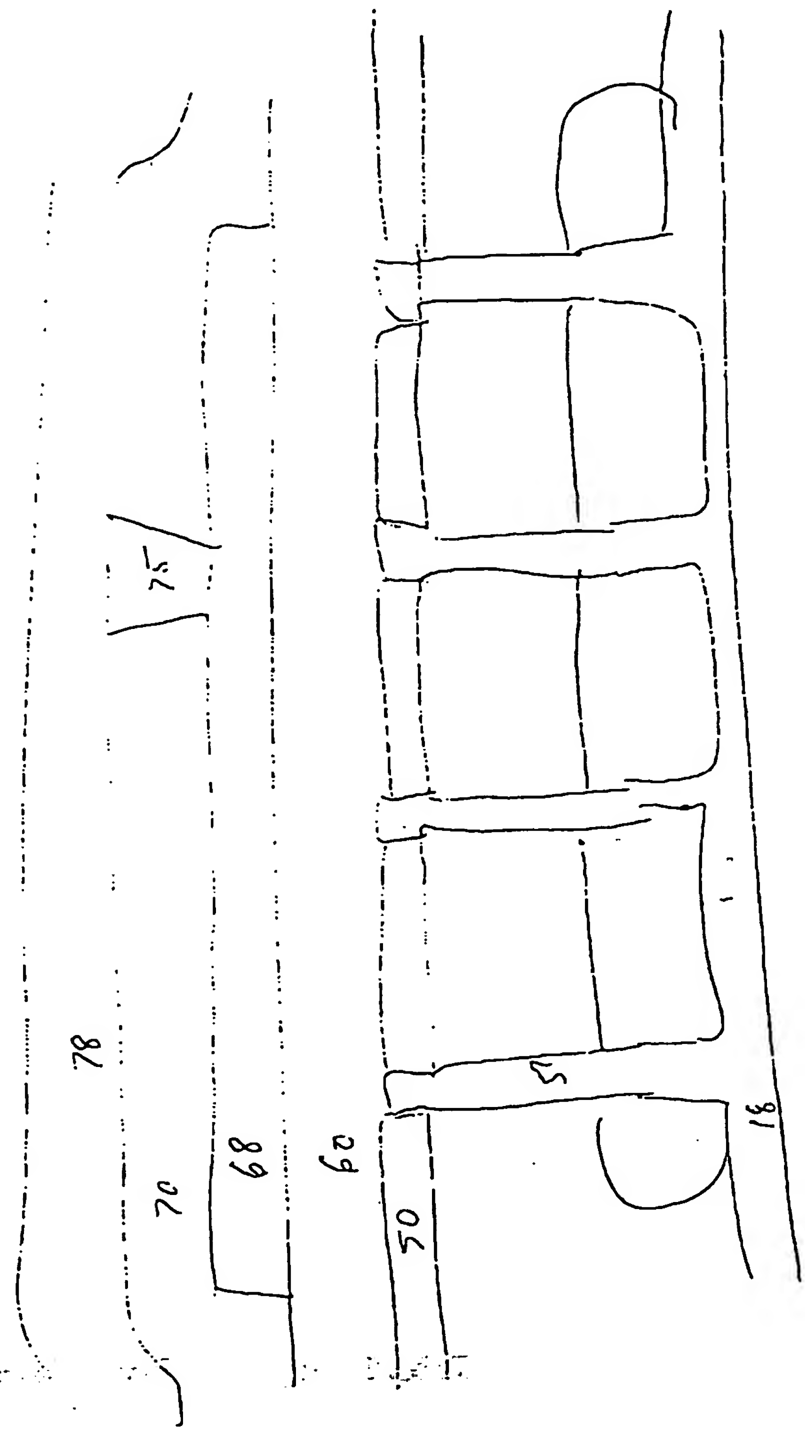


FIGURE 15

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 November 2000 (09.11.2000)

PCT

(10) International Publication Number
WO 00/67320 A3

(51) International Patent Classification[7]: H01L 23/64, 23/528

(21) International Application Number: PCT/US00/11798

(22) International Filing Date: 2 May 2000 (02.05.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/304,137 3 May 1999 (03.05.1999) US

(71) Applicant: SILICON WAVE, INC. [US/US]; 6256 Greenwich Drive, Suite 300, San Diego, CA 92122 (US).

(72) Inventors: SEEFELDT, James, Douglas; 4463 Meadowood Circle, DeForest, WI 53532 (US). HULL, Christopher, D.; 6534 Windward Ridge Way, San Diego, CA 92121 (US).

(74) Agents: BERG, Richard, P. et al.; Ladas & Parry, 5670 Wilshire Blvd., Suite 2100, Los Angeles, CA 90036 (US).

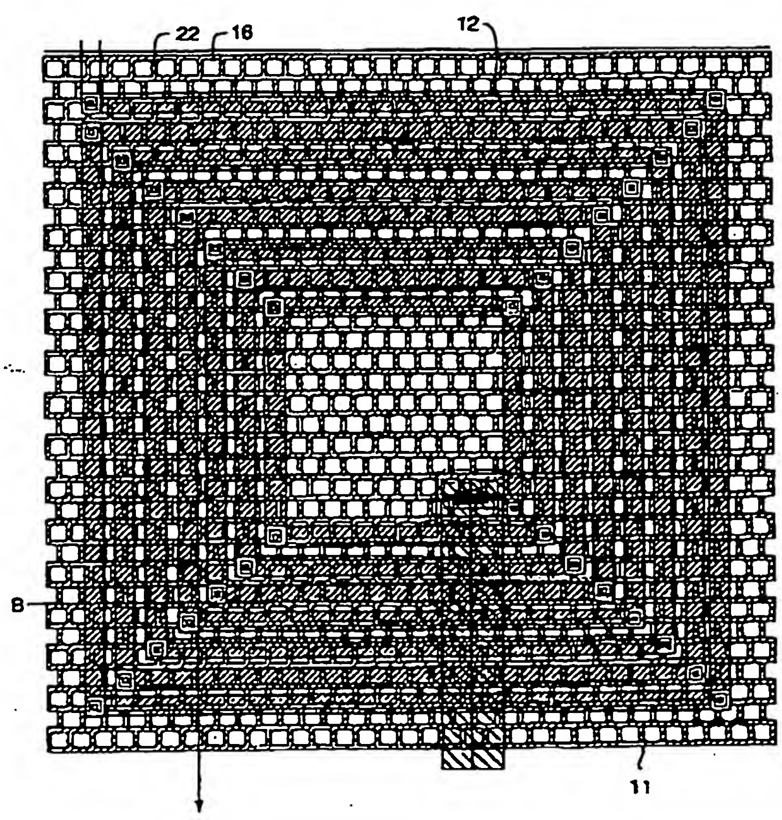
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *With international search report.*

[Continued on next page]

(54) Title: INTEGRATED CIRCUIT INDUCTOR WITH HIGH SELF-RESONANCE FREQUENCY



(57) Abstract: An integrated circuit inductor structure that includes a shielding pattern that induces a plurality of small eddy currents to shield the magnetic energy generated by the inductor from the substrate of the IC. The IC inductor structure is formed on a Silicon on Insulator (SOI) substrate where the substrate of the SOI has high resistivity. The shielding pattern forms a checkerboard pattern that includes a plurality of conducting regions completely isolated from each other by oxide material. The inductor has a high quality factor and a high self-resonance frequency due to the effective shielding of electromagnetic energy from the substrate of the IC while not reducing the effective inductance of the inductor.

WO 00/67320 A3

(88) Date of publication of the international search report: 31 May 2001

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/11798

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L23/64 H01L23/528

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	RONKAINEN H: "IC COMPATIBLE PLANAR INDUCTORS ON SILICON" IEE PROCEEDINGS: CIRCUITS DEVICES AND SYSTEMS,GB,INSTITUTION OF ELECTRICAL ENGINEERS, STENVENAGE, vol. 144, no. 1, 1 February 1997 (1997-02-01), pages 29-35, XP000692995 ISSN: 1350-2409 page 29, right-hand column, paragraph 3 -page 30, left-hand column, paragraph 2; figure 1	1-4
X	US 5 539 241 A (ABIDI ASAD A ET AL) 23 July 1996 (1996-07-23) cited in the application column 1, line 59 -column 2, line 3	1-4
A		5-15

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 November 2000	-7. DEZ. 2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Munnix, S

INTERNATIONAL SEARCH REPORT

I. [illegible]tional Application No
PCT/US 00/11798

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 03, 31 March 1999 (1999-03-31) -& JP 10 321802 A (TOSHIBA CORP), 4 December 1998 (1998-12-04) abstract paragraphs '0002!,'0009!-'0022!,'0040!,'0041! figures 1-4 ---	5-15
A	US 5 874 883 A (TAKAHASHI KIYOSHI ET AL) 23 February 1999 (1999-02-23) column 12, line 23 -column 13, line 57; figures 12,13 ----	5-15

INTERNATIONAL SEARCH REPORT	International application No. PCT/US 00/11798

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-4

   Integrated circuit comprising an inductor fabricated above a stack of dielectric layers contacting the surface of a substrate
   characterized in that said substrate has a high resistivity.

2. Claims: 5-15

   Integrated circuit, and method of manufacturing the same, comprising an inductor fabricated above a stack of dielectric layers contacting the surface of a substrate characterized in that an array of conductive regions inducing small eddy currents (e.g. by being spaced from one another by a dielectric) are located underneath the inductor and separated from it by a dielectric layer.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 00/11798

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5539241 A	23-07-1996	WO 9417558 A	04-08-1994
JP 10321802 A	04-12-1998	NONE	
US 5874883 A	23-02-1999	JP 9036312 A	07-02-1997

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 November 2000 (09.11.2000)

PCT

(10) International Publication Number
WO 00/67320 A3

(51) International Patent Classification[7]: H01L 23/64, 23/528

(21) International Application Number: PCT/US00/11798

(22) International Filing Date: 2 May 2000 (02.05.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/304,137 3 May 1999 (03.05.1999) US

(71) Applicant: SILICON WAVE, INC. [US/US]; 6256 Greenwich Drive, Suite 300, San Diego, CA 92122 (US).

(72) Inventors: SEEFELDT, James, Douglas; 4463 Meadowood Circle, DeForest, WI 53532 (US). HULL, Christopher, D.; 6534 Windward Ridge Way, San Diego, CA 92121 (US).

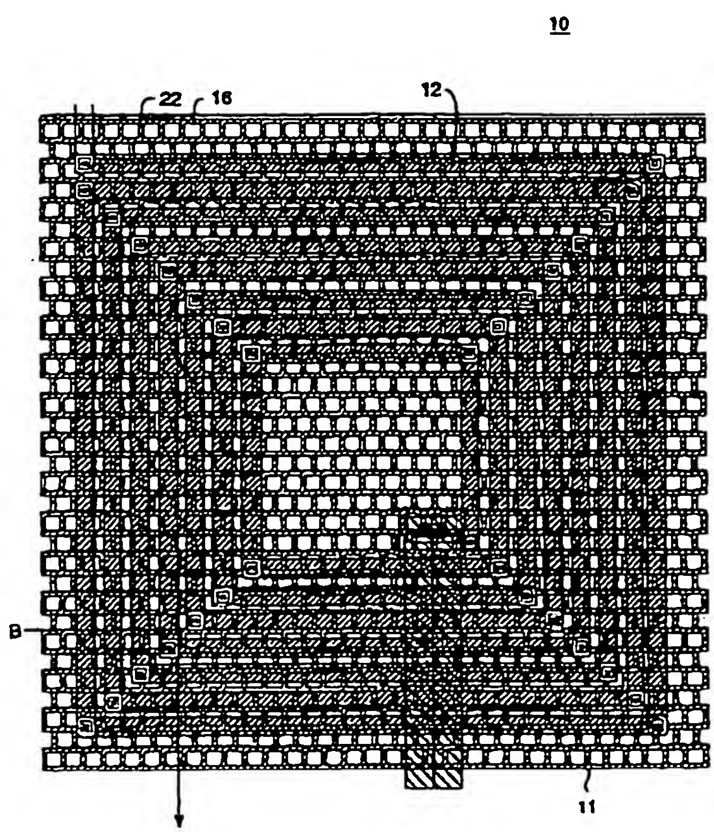
(74) Agents: BERG, Richard, P. et al.; Ladas & Parry, 5670 Wilshire Blvd., Suite 2100, Los Angeles, CA 90036 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: INTEGRATED CIRCUIT INDUCTOR WITH HIGH SELF-RESONANCE FREQUENCY



(57) Abstract: An integrated circuit inductor structure that includes a shielding pattern that induces a plurality of small eddy currents to shield the magnetic energy generated by the inductor from the substrate of the IC. The IC inductor strucure is formed on a Silicon on Insulator (SOI) substrate where the substrate of the SOI has high resistivity. The shielding pattern forms a checkerboard pattern that includes a plurality of conducting regions completely isolated from each other by oxide material. The inductor has a high quality factor and a high self-resonance frequency due to the effective shielding of electromagnetic energy from the substrate of the IC while not reducing the effective inductance of the inductor.

WO 00/67320 A3

Published:
— *with international search report*
— *with amended claims*

(88) Date of publication of the international search report: 31 May 2001

Date of publication of the amended claims: 26 July 2001

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

AMENDED CLAIMS

[received by the International Bureau on 07 February 2001 (07.02.01););
original claim 5 amended: remaining claims unchanged (1 page)]

1. An integrated circuit comprising:
   a) a high resistivity substrate;
   b) a first dielectric layer contacting the substrate at an interface;
   c) a second dielecuric layer contacting the first dielectric substrate at an interface; and
   d) an inductor fabricated above the second dielectric layer.

2. The integrated circuit according to claim1, wherein the resistivity of the substrate is about 1 kohm-cm.

3. The integrated circuit according to claim 1, wherein the first dielectric layer consists of silicon oxide.

4. The integrated circuit according to claim 3, wherein the second dielectric layer includes at least one oxide layer.

5. An integrated circuit comprising:
   a) a substrate;
   b) a first dielectric layer contacting the substrate at an interface;
   c) a second dielectric layer contacting the first dielectric layer at an interface, the second dielectric layer including a plurality of conducting regions
   d) a third dielectric layer contacting the second dielectric layer at an interface; and
   e) an inductor fabricated above the second dielectric layer,
   wherein the plurality of conducting regions induce small eddy currents that do not significantly reduce the inductance of the inductor.

6. The integrated circuit according to claim 5, wherein the substrate is a high resistivity substrate.